library ieee;

USE ieee.std\_logic\_1164.all;

USE ieee.numeric\_std.all;

Entity datamem\_test IS

END datamem\_test;

Architecture behavior of datamem\_test is

component datamem

port (

input : IN std\_logic\_vector(7 DOWNTO 0); --memd from Rx (register bank)

address : IN std\_logic\_vector(7 DOWNTO 0);--dAddress from Mux

aluop: in std\_logic\_vector(3 downto 0); -- opcode coming in

q : OUT std\_logic\_vector(7 DOWNTO 0);-- output

clk: std\_logic

);

END component;

signal input\_test : std\_logic\_vector (7 downto 0);

signal address\_test: std\_logic\_vector (7 downto 0);

signal aluop\_test: std\_logic\_vector (3 downto 0);

signal q\_test : std\_logic\_vector (7 downto 0);

signal clk\_test: std\_logic;

begin

test: datamem

Port map(input\_test,address\_test,aluop\_test,q\_test,clk\_test);

test1: input\_test<="00000010",

"10101010" after 40 ps;

test2: address\_test<="00000001",

"10101010" after 40 ps;

test3: aluop\_test<="1001" after 10 ps,

"1000" after 20 ps,

"1011" after 40 ps,

"1010" after 60 ps;

end behavior ;